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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,050	12/02/2003	Krishna Seshan	884-380US2	2687

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/726,050	SESHAN, KRISHNA	
	Examiner	Art Unit	
	Dao H Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *16-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1203*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 12/02/2003 through 08/30/2004, claims 1-29 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

a. Information Disclosure Statement (IDS) filed on 12/02/2003. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

b. Applicant made a provisional election without traverse to prosecute the invention of Group I, claims 1-15 and 28-29, drawn to a semiconductor device. Affirmation of this election was made in the Response to Restriction Requirement, and made of record as Paper dated 08/30/2004.

Applicant's comment about the grouping of claims 28 and 29 has been considered and are persuasive. Therefore, claims 28 and 29 have been re-grouped into Group I and being examined along with claims 1-15.

Claims 16-27 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group there being no allowable generic or linking claim.

Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

c. This application is a Divisional of the Patent Application No. 09/792,596 filed 02/23/2001, now Patent No. 6.686,659.

Specification

3. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim(s) 1-6, 13-15, and 28-29 is/are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 (lines 8-10) and 13 (lines 6-8), the limitations "wherein the at least one floating terminal comprises a ... solder bump, a ... conductor, and at least one dielectric layer physically separating and in physical contact with the ... solder bump and the ... conductor" is not clearly defined and distinctly pointed out the subject matter which is claimed as the Applicant's invention. It is not clear of how the dielectric layer being physically separating and also in physical contact with both of the solder bump and the conductor?

Claims (2-6, 28-29), and (14-15) depend from rejected base claims 1, 13 respectively, and include all of the limitations of claims 1, 13, thereby rendering these dependent claims indefinite.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim(s) 1-5 and 28-29 is/are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 4,439,813 by Dougherty et al.

Regarding claim 1, Dougherty discloses an integrated circuit (IC), as shown in figures 1-4, comprising:

at least one circuit element, a node coupled to the at least one circuit element (these are inherent since the solder ball or the terminal must be connected to a circuit element to provide input/output for it);

at least one non-floating terminal (fig. 1A, left solder ball combination) on a surface of the IC to mount to a corresponding pad on the substrate, wherein the at least one non-floating terminal comprises a first solder bump and a first conductor (fig. 2);

at least one floating terminal (fig. 1A, right solder ball combination) on the surface of the IC to mount to a corresponding pad on the substrate, wherein the at least one floating terminal comprises a second solder bump, a second conductor, and at least one dielectric layer; and

at least one coupling element to couple any combination of the at least one floating terminal and the at least one non-floating terminal to the node. See figs. 1.

Regarding claim 2, Dougherty discloses the IC wherein the node is from the group consisting of power nodes, ground nodes, and input/output nodes. This is inherent.

Regarding claim 3, Dougherty discloses the IC wherein the second solder bum, second conductor, and at least one dielectric layer If the at least one floating terminal form a capacitive element. See figs. 1 and col. 5, line 1-10.

Regarding claim 4, Dougherty discloses the IC wherein the first conductor and the second conductor can be selectively coupled to the node. See fig. 1A and col. 2, lines 25-46; col. 5, lines 10-37.

Regarding claim 5, Dougherty discloses the IC wherein the substrate pad is selected from the group consisting of a power terminal, a ground terminal, and an input/output terminal connector. See fig. 1A.

Regarding claims 28-29, Dougherty discloses the IC comprising all claimed limitations. These are all inherent limitations, depending on each specific design.

Claim Rejections - 35 U.S.C. § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim(s) 6-15 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 4,439,813 to Dougherty et al., in view of Bertin et al., U.S. Patent No. 6,255,899.

Regarding claim 6, Dougherty discloses the IC comprising all claimed limitations, except for the coupling element comprising selector logic coupled to the at least one floating terminal, to the at least one non-floating terminal, and to the node, and comprising at least one control input, at least one logic element coupled to the at least one control input, and at least one output to couple any combination of the first and second conductors to the node.

Bertin discloses an assembly a logic element, as shown in figs. 1(A-B), comprising decoupling capacitor 122(a-c) and control logic element 120.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Dougherty so that it would also include a control logic element as that of Bertin to drive a particular signal line. See col. 1, lines 63-67 of Bertin.

Regarding claim 7, Dougherty discloses an integrated circuit (IC), as shown in figs. 1-4, comprising:

a plurality of circuit elements, a plurality of nodes coupled to the plurality of circuit elements (fig. 1; col. 2, lines 26-64);

a plurality of non-floating terminals (fig. 1A: left solder ball combination) on a surface of the IC;

at least one floating terminal (fig. 1A: right solder ball combination) on the surface of the IC.

Dougherty is silent about a selector logic coupled to the terminals and to the plurality of nodes to couple any combination of the at least one floating terminal and one of the plurality of non-floating terminals to one of the plurality of nodes.

Bertin discloses an assembly a logic element, as shown in figs. 1(A-B), comprising decoupling capacitor 122(a-c) and control logic element 120.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Dougherty so that it would also include a control logic element as that of Bertin to drive a particular signal line. See col. 1, lines 63-67 of Bertin.

Regarding claims 8-11, Dougherty/Bertin discloses the device comprising all claimed limitations. See figs. 1 of Dougherty.

Regarding claim 12, Dougherty/Bertin discloses the IC wherein the selector logic comprises at least one control input and further comprises at least one output to selectively couple any combination of the at least one floating terminal and one of the plurality of non-floating terminals to the one node. See figs. 1, and 3-4 of Bertin.

Regarding claim 13, Dougherty discloses an electronic assembly, as shown in figs. 1-4, comprising:

an integrated circuit (1C) comprising at least one circuit element, a node coupled to the at least one circuit element (these are inherent since the solder ball or the terminal must be connected to a circuit element to provide input/output for it);

at least one floating terminal (fig. 1A, right solder ball combination) on the surface of the IC to mount to a corresponding pad on a substrate, wherein the at least one floating terminal comprises a solder bump (solder ball), a conductor (top metallurgy), and at least one dielectric layer (high k dielectric); and

an IC package substrate comprising a plurality of pads and internal circuit paths, including at least one pad and at least one internal circuit path to couple to the at least one floating terminal.

Dougherty is silent about a coupling element to switchably couple the at least one floating terminal to the node.

Bertin discloses an assembly a logic element, as shown in figs. 1(A-B), comprising decoupling capacitor 122(a-c) and control logic element 120 which is switchably coupling various element to each other.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Dougherty so that it would also include a control logic element as that of Bertin to drive a particular signal line. See col. 1, lines 63-67 of Bertin.

Regarding claim 14, Dougherty discloses the electronic assembly wherein the solder bump, conductor, and at least one dielectric layer form a capacitive element. See fig. 1.

Regarding claim 15, Dougherty/Bertin disclose the device comprising all claimed limitations. See figs. 1 and 3-4 of Bertin.

Conclusion

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
October 28, 2004